second section, doping concentration in each of the first and second sections increasing with distance from the upper surface;

forming first and second trenches in the epitaxial layer that extend vertically from the upper surface down into the substrate to define a mesa having first and second sidewalls, the first and second sections comprising a drift region of the mesa;

forming a dielectric layer over the first and second sidewalls;

forming source and body regions in an upper portion of the mesa, the source region being of the first conductivity type and the body region being of a second conductivity type opposite to the first conductivity type, the body region separating the source from the first section of the drift region; and

forming a gate embedded within the dielectric layer adjacent the body region.

2. The method of claim **1** further comprising:

forming a source electrode connected to the source region; and

forming a drain electrode connected to the substrate.

3. The method of claim **1** wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type.

4. The method of claim **1** wherein the forming of the dielectric layer partially fills each of the trenches, and further comprising filling a remaining portion of the first and second trenches with a conductive material.

5. The method of claim **1** wherein the dielectric layer comprises an oxide.

6. The method of claim **1** wherein the conductive material comprises doped polysilicon.

7. A method of fabricating a power transistor comprising:

forming an epitaxial layer with a doping concentration gradient that varies in a lower portion of the epitaxial layer, the doping concentration gradient in the lower portion increasing with vertical distance from an upper surface of the epitaxial layer, the doping concentration gradient differing by at least 10% from near a top of the lower portion to near a bottom of the lower portion;

forming first and second trenches in the epitaxial layer that extend vertically from the upper surface to define a mesa having first and second lateral sidewalls, the lower portion comprising a drift region of the mesa;

covering the first and second sidewalls of the mesa with a dielectric material; and

forming a trench gate structure embedded within the dielectric material laterally adjacent an upper portion of the mesa.

8. The method of claim **7** wherein the epitaxial layer is formed with a first conductivity type.

9. The method of claim **8** further comprising:

forming source and body regions in the upper portion of the mesa, the source region being of the first conductivity type and the body region being of a second conductivity type opposite to the first conductivity type, the body region separating the source from the lower portion of the drift region.

10. The method of claim **7** further comprising forming first and second field plate members in the first and second trenches, respectively, the first and second field plate members being formed of a conductive material fully insulated from the mesa by the dielectric material.

11. A method of fabricating a power transistor comprising:

forming an epitaxial layer with a doping concentration gradient that varies in a vertical direction through a lower portion of the epitaxial layer by at least 10% from near a top of the lower portion to near a bottom of the lower portion, the doping concentration gradient increasing with distance from an upper surface of the epitaxial layer;

forming first and second trenches in the epitaxial layer that extend vertically from the upper surface to define a mesa, a lower portion of the mesa comprising a drift region;

forming first and second field plate members in the first and second trenches, respectively, the first and second field plate members being formed of a conductive material fully insulated from the mesa by a dielectric material;

forming source and body regions in an upper portion of the mesa, the source region being of a first conductivity type and the body region being of a second conductivity type opposite to the first conductivity type, the body region separating the source from the drift region, the drift region being of the first conductivity type;

forming a gate embedded within the dielectric material adjacent the body region; and

electrically coupling the source region with the first and second field plate members.

12. The method of claim **11** further comprising forming a drain electrode electrically coupled to the drift region.

13. The method of claim **11** wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type.

14. The method of claim **11** wherein the forming of first and second field plate members comprises forming a layer of the dielectric material in each of the first and second trenches, the layer covering first and second sidewall portions of the mesa.

15. The method of claim **11** wherein the dielectric material comprises silicon dioxide.

16. The method of claim **11** wherein the conductive material comprises doped polysilicon.

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